IN THE U.S. PATENT AND TRADEMARK OFFICE

In re Application of

Takahashi, Hiroshi

Serial No.: **09/884,662**

Filed: **06/19/2001**

Docket No.: **TI-29232**

Art Unit: **2819**

Examiner: **Chang, Daniel**

Conf. No.: **4499**

For: **HIGH SPEED SEMICONDUCTOR CIRCUIT HAVING LOW POWER CONSUMPTION**

AMENDMENT TRANSMITTAL FORM

Assistant Commissioner For Patents

Washington, D.C. 20231

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(a)

I hereby certify, that on this date, this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, DC 20231.

Elizabeth Austin — Date 3/4/2003

Sir:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated as shown below:

CLAIMS AS AMENDED						
	CLAIMS REMAINING AFTER AMENDMENT		**HIGHEST NUMBER PREVIOUSLY PAID FOR**	**PRESENT EXTRA**	**RATE**	**ADDITIONAL FEE**
Total Claims	27	Minus	27	0	x $18 =	$ 0.00
Independent Claims	3	Minus	3	0	x $84 =	$ 0.00
					TOTAL ADDITIONAL FEE	$ 0.00

Charge the total additional fee, and any further fees, or credit overpayment to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. An original and two copies of this sheet are enclosed.

Texas Instruments Incorporated
P. O. Box 655474, M/S 3999
Dallas, TX 75265
Ph: (972) 917-5299
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Attorney for Applicants
Reg. No. 34,227

Response under 37 C.F.R. § 1.116
Expedited Procedure
Examining Group 2819

10/13 Amdt
3-17-03
A.Wall

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AMENDMENT - 37 CFR § 1.116

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Elizabeth Austin — Date 3/4/2003

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

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Responsive to the Office Action dated September 24, 2002, please amend the above identified application as follows:

IN THE CLAIMS – (clean version):

sub C1 7

1. (twice amended) A semiconductor device, comprising:

a logic circuit, which includes a MOS transistor, and

a bias voltage supply circuit, comprising no more than two transistors each having its gate coupled to receive a control signal the logical reverse of the control signal received by the other transistor, which selectively supplies a first bias voltage or a second

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